DFI Lanparty LT X38-T2R

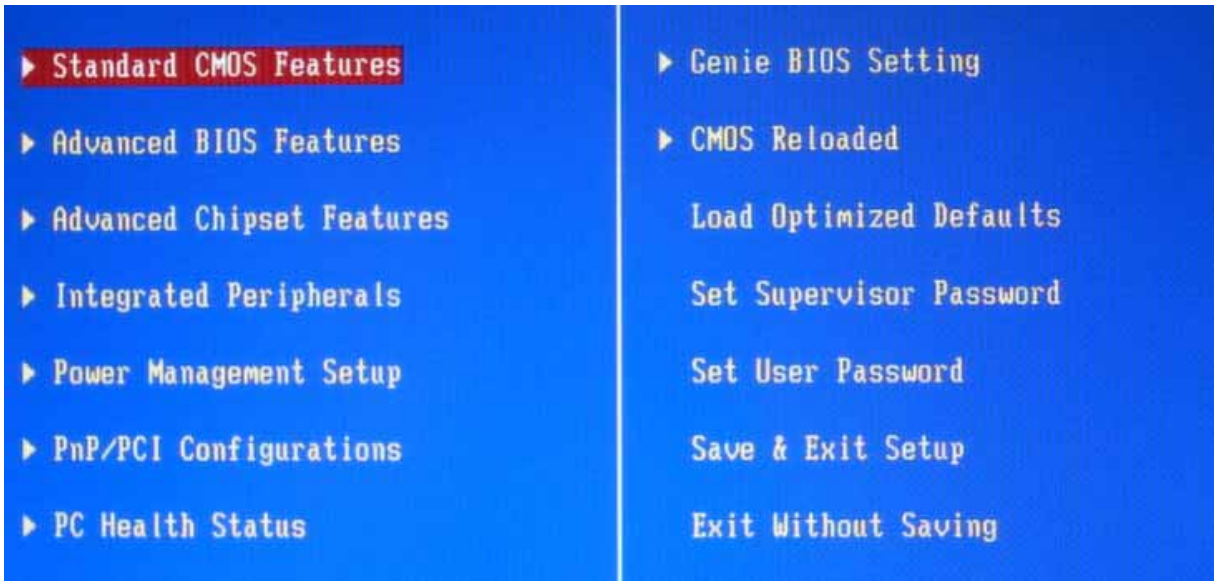
BIOS Setting Guideline

(BIOS version: 2007/1/11) V001

- Pressing **DEL** at DFI LT X38 LOG screen to login BIOS setup screen

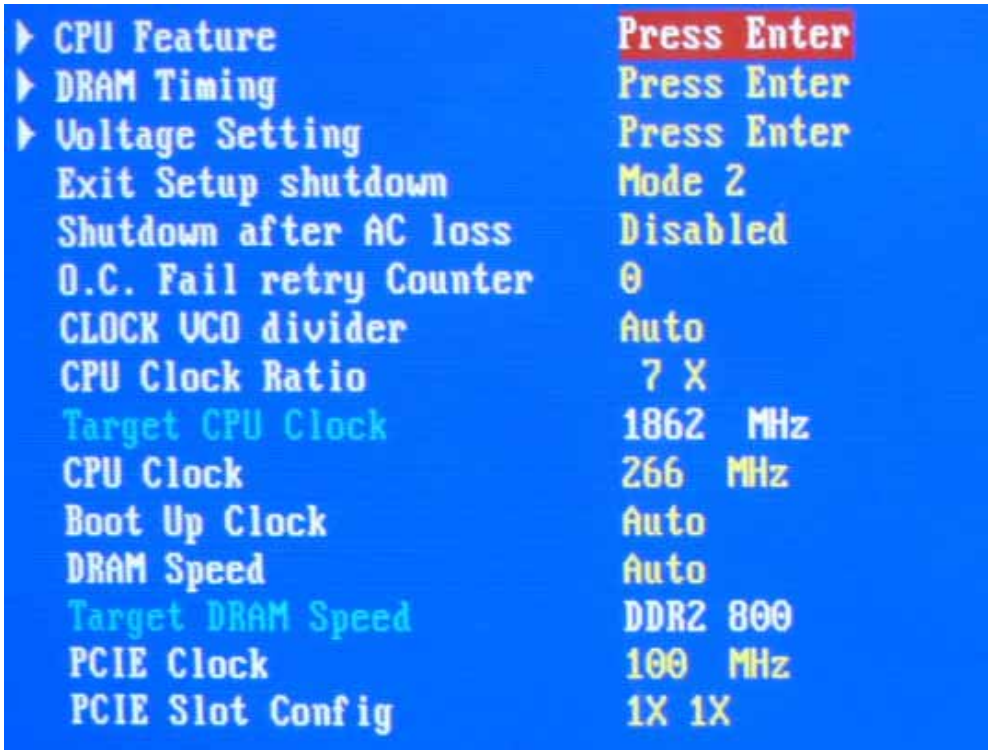
- BIOS setup screen

L



➢ Genie BIOS settings: *This setup thread is combined all needed settings for over clocking (CPU speed setting, CPU features, DRAM timings, Voltage settings and PCI speed etc.)*

➢ Genie BIOS : *Main setup screen*



Exist Setup Shutdown: Mode1/Mode2

Somehow it's a "characteristic" of Intel chipset when overclocking… it will shutdown after tweaking. For that, DFI has 2 different modes to chose:

Mode 1) when the system was boot-up, it will run a little "diagnose".

If the CPU frequency doesn't change too much, it will skip the "shutdown" function and rewrite the clock generator directly.

Mode 2) no matter how little the CPU clock or DRAM's ratio has been changed,

The system still "shutdown" and reboot by itself

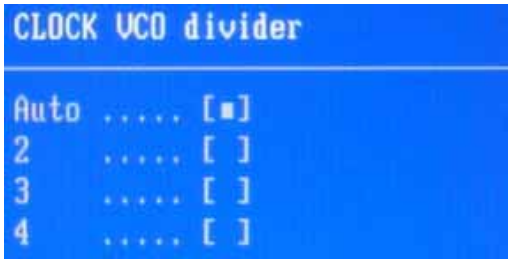
Shutdown after AC Loss: Enable/Disable

System Power recovers item. (Enabled for power on system automatically if AC power failure)

OC Fail Retry Counter: 0~3 times

OC fail retry looping setting. For example, set it on 1, it will retry boot again if fail, then **auto back CPU default** value to boot system.

Clock VCO Divider: Auto / 2 / 3 / 4

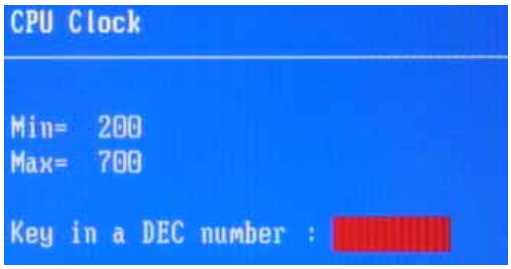


This function is use to fix the clock generator's divider and "NB Strap" by its jumper. Then, system wouldn't be reboot again because it presumed itself is not in an overclock status. (This function needs to cooperate with particular jumper)

CPU Clock ratio:

CPU multiplier setting, **6~11** for locked processors, **6~50** times for unlocked processors

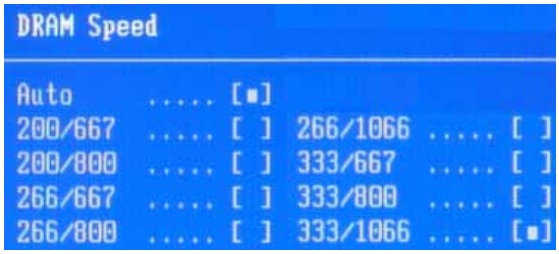
CPU Clock range:



Boot-up clock: Auto/ 100MHz ~410MHz

This function can help you out for setting a lower boot up clock. As a buffer, when your FSB is tweaked too high in the beginning. The process will to be: system boot up with "Boot-up clock" first, after that it will change to your highest FSB.

DRAM Speed:



PCIE Slot Config:

PCIE 2 and PCIE 4 transferring status:

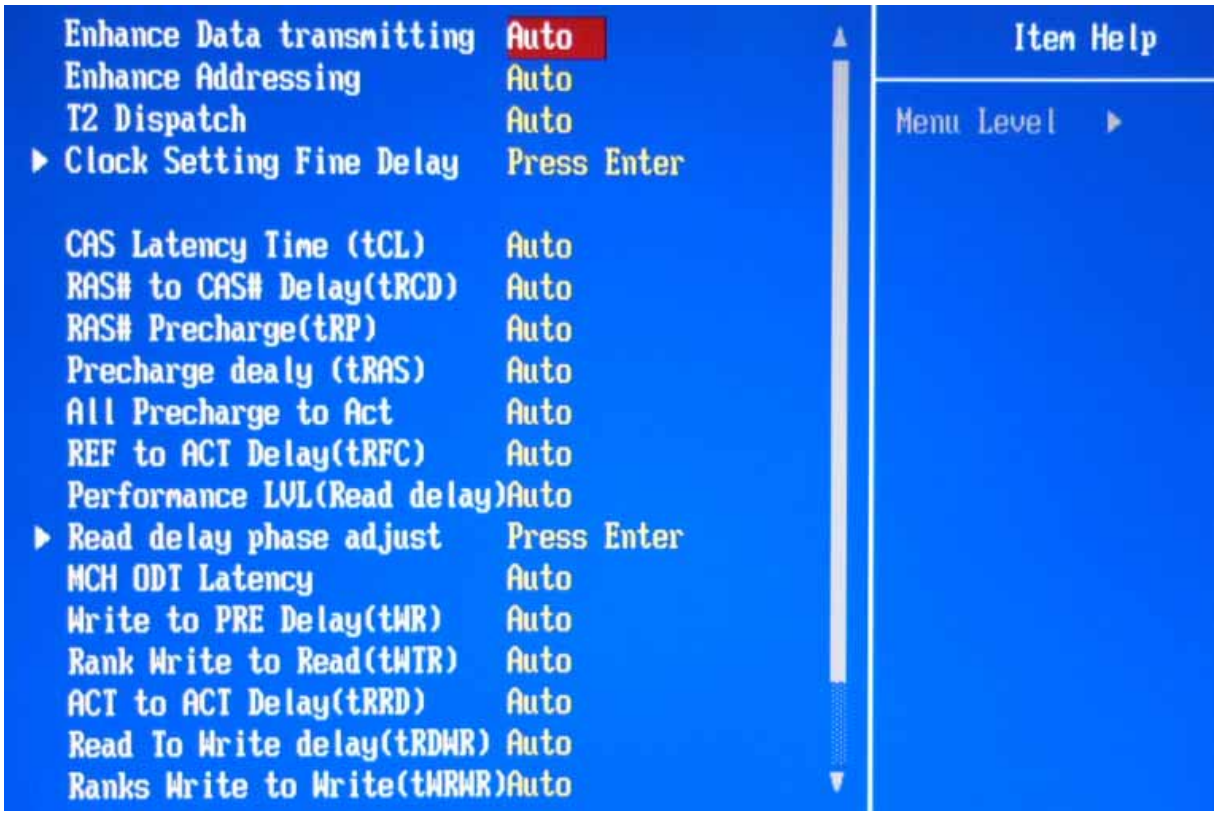
1X 1X : PCIE 2 / 4 are running with 1X model

4X NC: PCIE4 is running 4X mode, PCIE 2 will be disable and on board ***LAN2 will be disable as well.***

➢ CPU Feature:

(For gaining a maximum CPU utilization, we will always disable all CPU key features except “Core multi-Processing”)

➢ DRAM Timing:



Enhance Data Transmitting: Auto / Normal / First / Turbo

DFI specifically designed a “fine-tune mode” for DATA transmitting performance, Normal for lowest performance, Fast for highest performance, Default AUTO will automatically adjust performance based on current system Front Side BIOS.

Enhance Addressing: Auto / Normal / First

DFI specifically designed a “fine-tune mode” for DATA addressing, “Normal” for lowest performance, “Fast” for highest performance, Default AUTO will automatically adjust performance based on current system Front Side BIOS.

T2 Dispatch: Auto/ Enabled / Disabled

DRAM performance parameters patch, enabling for getting optimized and disabling to relax DRAM timing for running higher working frequency on modules.

Performance level:

It is tRD of DRAM parameter

Read delay phase adjust:

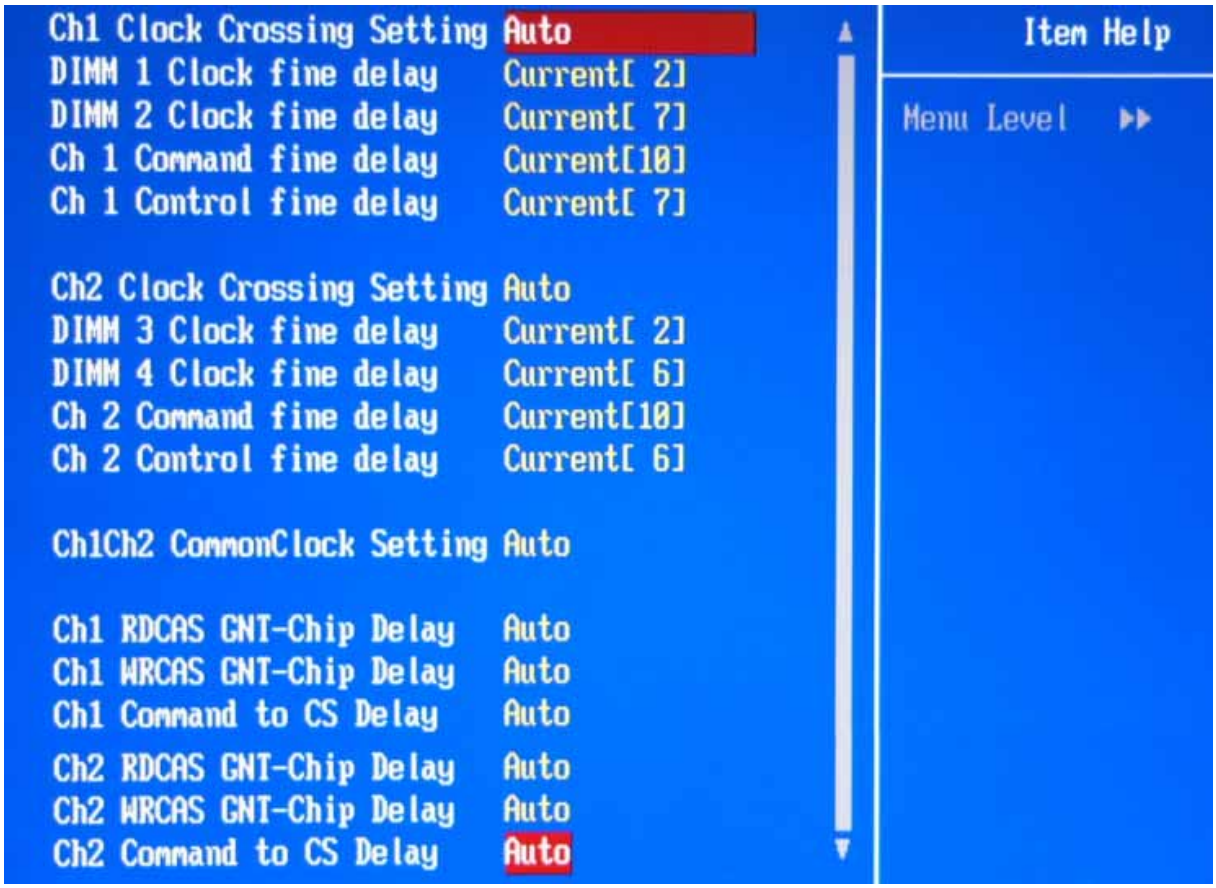
It is the fine-tune feature for tRD

MCH ODT Latency:

DRAM ODT read/Write latency,

(Basically ODT is On Die Termination, it likes a variable resistor termination to protect DATA signal integrity from high frequency interference)

➢ CLK setting fine delay:



Ch1 / Ch2 Clock Crossing Setting :

Auto / More aggressive /aggressive / Nominal / Relaxed / More Relaxed

Giving an easy explanation, after the CPU, PCIE, DRAM locked the clock phase by “PLL phase locked loop”, we can utilize the DRAM DLL to adjust DRAM operating phase by tuning DRAM DATA output phase forward or backward to create a better match with current DATA operating phase.
The BIOS will automatically calculate a parameter after system boot up.
The BIOS will show the current value of this parameter.
The best tuning range for finding the best DATA operating phase will be 3 ranks before or after this current value.

Ch1Ch2 CommonClock Setting:

Auto / More aggressive /aggressive / Nominal / Relaxed / More Relaxed

As above, it is PLL fine-tune for Common clock signals of DRAM modules.

Ch1/Ch2 RDCAS GNT-Chip Delay: Auto /1~7 CLK

Read command rate, 1Clock is Intel Command rate **1N** mode, 2~7Clock are **1N disable** mode

Ch1/Ch2 WRCAS GNT-Chip Delay: Auto /1~7 CLK

Write command rate, 1Clock is Intel Command rate **1N** mode, 2~7Clock are **1N disable** mode

Ch1/Ch2 Command to CS Delay: Auto /1~7 CLK

DRAM module bank selecting command rate, 1Clock is Intel Command rate **1N** mode, 2~7Clock are **1N disable** mode

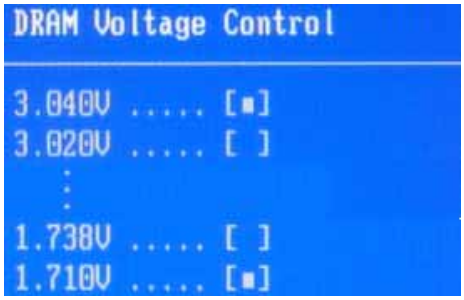
---

➢ Voltage Settings:

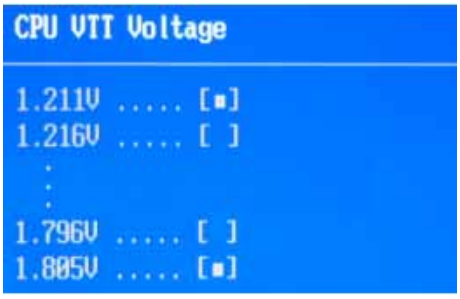
CPU VID Control range:

CPU VID Special Add:

DRAM Voltage range:



CPU VTT Voltage range:



SB Core / CPU PLL voltage: (1.51V~2.38V)

These two voltages are controlling by same adjustable circuit, increasing CPU PLL voltage higher is better for gaining a stable OC situation.

NB Core Voltage: (1.265V~2.040V)

Vcore drop control: **Enable / Disabled**

Enabling to control Vout level by PWM, disabling to get a maximum output.

Clockgen voltage control: (3.45V~3.85V)

Clock working voltage, increase it to achieve higher and more stable in extreme FSB environment

GTL+ buffer Strength: **Strong / Weak**

It is adjustment option for North-Bridge reference voltage strength.

Host Slew Rate: **Strong / Weak**

It is adjustment option for North-Bridge voltage driving strength.

GTL REF Voltage control: **Enable / Disabled**

CPU VTT reference voltage for determining host bus high / low level.

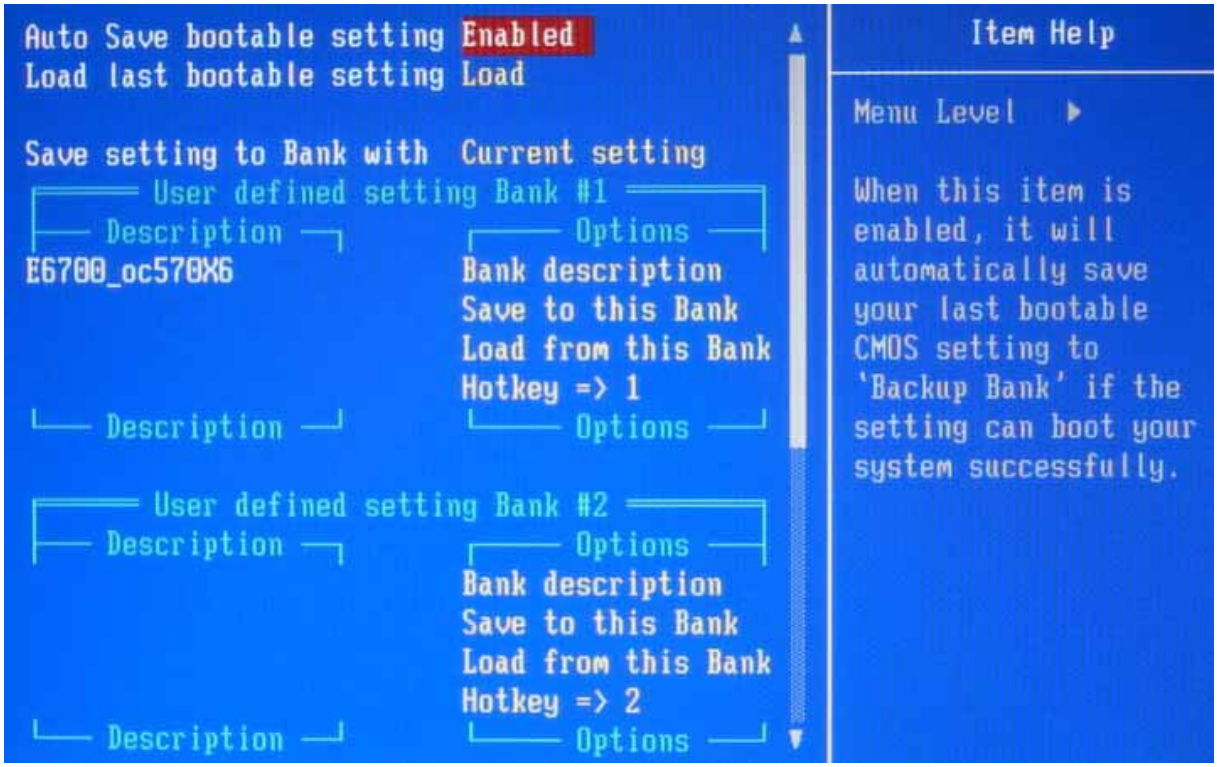
➢ Manual GTL Voltage Table:

VTT (Real)	CPU GTL 1/2 REF (Real)	CPU GTL 0/3 REF (Real)	NB GTL REF.(Real)
1.100V (1.060V)	95 (0.711V)	90 (0.713V)	75 (0.716V)
1.250V (1.213V)	110 (0.812V)	105 (0.816V)	85 (0.812V)
1.35V (1.310V)	120 (0.878V)	110 (0.875V)	90 (0.873V)
1.453V (1.411V)	130 (0.947V)	120 (0.945V)	100 (0.945V)
1.553V(1.508V)	140 (1.014V)	130 (1.014V)	110 (1.015V)
1.603V (1.550V)	140 (1.038V)	130 (1.037V)	110 (1.041V)
GTL REF voltage definition= 0.67% VTT, Please choose a correct value for VTT when "GTL REF Voltage" item was selected on Manual.			

For details, please link to: http://dfics.dfi.com.tw/dfi_cs/LTX48/X38X48_vtt.xls

---

➢ BIOS Reloaded function: *DFI Lan Party series are providing 1last fine status + 4 user's profile space for doing BIOS setting saving and recovery*.



Auto Save bootable setting: Enable / Disable

For saving last fine/ bootable parameters by BIOS itself every time

Load last bootable:

For loading last BIOS parameters.

Save setting to bank with: Current settings or last saved CMOS settings.

To define the resource of parameters for bank saving.

User define setting bank #1 ~ #4:

1. Bank Description: There are 4 rows for writing a short description. Double click on row when this row is empty, it will erase pervious data.

2. Save to this bank: Press "Y" to save data to this bank
3. Load from this bank: Press "Y" to load data of this bank to be current BIOS setup settings.
4. Hotkey =>: define the "hotkey" for a quick change BIOS settings to boot. Please press Hotkey after power on system immediately.

➢ EZ Clear CMOS methods:

a. To press *POWER + Reset bottoms* for 5sec when 5Vsb existed, by doing that current CMOS data will be clear

b. To *hold Home key* to power on system, BIOS will recover FSB to default, remains setting will be keeping the last time fine status.

c. To *hold Insert key* to power on system, BIOS will load all setting back to default as like doing a CCMOS by manually.

End